GEORGE O. SAILE & ASSOCIATES
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

FACSIMILE TRANSMITTAL SHEET

TO: Examiner Tan N Tran	FROM: Stephen B. Ackerman
DEPT:	DATE: June 7, 2004
COMPANY: US Patent & Trademark Office	FAX NUMBER: 845 471 2064
FAX NUMBER: 571 273 1923	PHONE NUMBER: 845 452 5863
RE: 10/042,074	# OF PAGES 4

NOTES/COMMENTS:

Please enter it,

Dear Examiner Tran,

Per the earlier telephone conversation of today, attached is a Proposed Amendment to provide support in the Specification for what is claimed, and to describe some of the claim elements' relationship to Fig. 6.

With Best Regards,

Stephen B. Ackerman, Reg. No. 37,761

Proposed Amendment

Please replace the paragraph beginning on page 6 line 9 with the following paragraph:

The structure of a preferred embodiment of the new grid metal design for CMOS image sensor chips is shown in Fig. 5, which depicts the layout and in Fig. 6, in which is shown the layered structure of the pixel area. In the new grid metal design the photodiode peripheral areas, which in the conventional design, 50, are sparsely covered by two levels, 26 and 28, of interconnection metal, are completely covered by additional full levels of metal, 52. As in conventional CMOS image sensor chips the image pixel area, 20 can occupy about 90% of the chip area. This area, usually arranged in the form of a grid matrix array as shown, contains photodiode regions, 48, which take up most of the area and the remaining sensor circuitry, which are placed in the areas 50, peripheral to the photodiodes. Logic circuits are contained in the chip peripheral area, 22, which also contains metal regions, 24. Dummy metal patterns are added to completely cover the region peripheral to the photodiodes. These dummy metal patterns are therefore disposed over the functional metal levels of the image sensors and over the image sensor circuit elements other than the photodiode, these features being placed in the regions peripheral to the photodiodes. Generally, only two levels of metal are used, for interconnection, in the image pixel regions, while five levels of metal<u>, shown in Fig.6 as 80, 82, 84, 86 and 88,</u> are often required for the logic circuits<u>, 90,</u> placed in the chip peripheral area. Three levels of metal are thus available, essentially for free, for the dummy metal patterns in the image pixel region, and these are the three metal levels, 56,58 and 60 are the dummy

Proposed Amendment

patterns of preferred embodiments of the invention. The area of the dummy metal patterns is much larger than that of the metal levels of the peripheral logic circuits. The exposed surface area of the dummy metal levels does not change appreciably during metal etch and consequently there is only a small fractional change during metal etch in the exposed metal surface area of the chip. The loading affects during metal etching are therefore alleviated. With complete metal coverage of the photodiode peripheral regions, the image sensor circuits other than the photodiodes, which are contained in these regions, are well shielded from the incoming light. In a conventional CMOS image sensor the pixel interconnection metal levels do not completely shield the underlying sensor devices from incoming light, which can result in extraneous currents and noise that affects the performance of the devices. With the new grid metal design of the invention, which includes complete metal coverage of the photodiode peripheral regions that shields the sensor devices from incoming light, these extraneous current and noise are not generated. Furthermore, the two interconnection metal levels are insufficient to adequately collimate incoming light and there is cross talk to nearby sensors, as indicated in Fig.4, 46. In preferred embodiments of the invention three dummy metal patterns are added to the two functional metal levels in the image pixel regions. These provide five levels of metal that adequately collimate incoming light and prevent cross talk to nearby sensors, as indicated in Fig.6. <u>In preferred embodiments depicted in Fig.6 the first two metal levels are functional in both the image pixel regions and in the chip peripheral area. Such metal levels are denoted levels of the first type. Thus regions 26 and 88, which make up the first metal level, are constituents of a metal level of the first type.</u>

Proposed Amendment

Similarly, regions 28 and 86, which make up the second metal level, are constituents of a metal level of the first type. In preferred embodiments depicted in Fig.6 metal levels 3, 4 and 5 are not functional in the image pixel regions. Such metal levels are denoted levels of the second type. Thus regions 56 and 84, which make up the third metal level, are constituents of a metal level of the second type. In this case region 84 happens to be functional, it would be a metal level of the second type even if it were not functional. Similarly, regions 58 and 82, which make up the fourth metal level, are constituents of a metal level of the second type, and also regions 60 and 80, which make up the fifth metal level, are constituents of a metal level of the second type .